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Message : Re: Our Docket No. 55561 (70820)
U.S. Serial No. 09/775,167

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Docket No. 55561 (70820)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Y. Kubota et al.		
U.S. SERIAL NO.:	09/775,167	GROUP:	2675
FILED:	February 1, 2001	EXAMINER:	A. Nelson
FOR:	SHIFT REGISTER CIRCUIT CAPABLE OF REDUCING CONSUMPTION OF POWER WITH REDUCED CAPACITIVE LOAD OF CLOCK SIGNAL LINE AND IMAGE DISPLAY DEVICE INCLUDING IT		

CERTIFICATE OF FACSIMILE TRANSMISSION

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By: _____
Steven M. Jensen

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated October 14, 2005 of the above-referenced application. A request for a one-month extension of time is submitted herewith. Applicants respond to the Office Action as follows.

Claims 1-25 are pending in the application.

Independent claims 1 and 25 recite a shift register circuit including: a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal, the plurality of register blocks being serially connected together; and a **transfer gate** for controlling the clock

signal supplied to the flip-flop, the transfer gate of a corresponding register block being brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes (see, e.g., claim 1).

In other words, as recited in independent claims 1 and 25, the clock signal is inputted into the flip-flop through the transfer gate. By using the transfer gate, which has a smaller input load capacitance than a logic gate, the Applicants' claimed shift register circuit can reduce power consumption, as compared to the prior art.

Claims 1 and 25 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,289,518 to Nakao. The remaining claims were rejected over prior art including the Nakao reference. These rejections are respectfully traversed.

The Nakao reference is directed to a low power shift register circuit for "lowering the power consumption by means of reducing an idle current flowing through the logic circuit" (see column 1, lines 63-66). Referring to FIG. 4, four flip-flops 31, 32, 33, and 34 are connected in series and synchronized with clock signals. The output terminal of a NAND gate 51 is connected to a clock-signal input terminal CKT of the flip-flop 31 (see column 3, lines 43-45). When a high-level data signal is input to the flip-flop 31, an exclusive OR gate 61 supplies a high-level input signal N1 to the NAND gate 51, and the clock signal is input to the flip-flop 31 (see column 3, line 64 to column 4, line 3). Subsequently, at timing T2, the output signal Q1 is at a high level, and the exclusive OR gate 61 outputs a low-level signal N1, where the clock signal is not supplied to the flip-flop 31 (see column 4, lines 8-14).

In Nakao, the output signal Q1 is compared to the input data signal, and if these signals are at the same logic level, the clock signal is blocked by the NAND gate 51 (see column 4, lines 14-18). Only when these signals are different is the clock signal input to the flip-flop 31.

In the Office Action of 10/14/2005, the NAND gate 51 and clock signal CK1 were cited as allegedly corresponding to Applicants' claimed **transfer gate**.

Nakao does not teach or suggest "a transfer gate for controlling the clock signal supplied to the flip-flip," as recited in independent claims 1 and 25.

In Nakao, the clock signal CK1 is inputted into a flip-flop 31 through a NAND gate 51, which is a type of logic gate. Applicants' claimed invention requires use of a **transfer gate**, which has an input load capacitance smaller than a logic gate, and thus reduces power consumption as compared to the circuit disclosed in Nakao. Therefore, the NAND gate 51 in Nakao is not equivalent to Applicants' claimed "transfer gate."

Moreover, Nakao does not teach or suggest a shift register circuit in which the transfer gate of a corresponding register block/flip-flop is brought into an ON-state only in a specified period when an output of the corresponding register block/flip-flop changes.

For example, referring to FIG. 5 of Nakao, the output signal N1 (inverse of clock signal CK1) is high **before** the corresponding output signal Q1 is high. Then, at time T1, when the output signal Q1 becomes high, the output signal N1 is low. Therefore, changes in the output signal N1 (and hence, the clock signal CK1) precede any changes in the output signal Q1. Accordingly, Nakao does not teach or suggest a shift register circuit in which a transfer gate is turned ON *only when an output of the flip-flop changes*.

For at least the reasons discussed above, the Nakao reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed that the claims are now in condition for allowance. However, if there are any outstanding issues, the Examiner is urged to call the Applicants' representative at the telephone number listed below.

Applicants believe that additional fees are not required for consideration of the within response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

Date: February 14, 2006

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